IN THE CLAIMS

1. (Cancel)

2. A method of multichannel analog/digital (A/D) conversion, in which in a first and second channel respectively in a first or second channel provision area a first and second analog signal awaiting conversion is sampled by a respective first and second S/H (Sample & Hold) element and the respectively stored sample value thereof is applied as a channel sample to a first and second input of an analog multiplexer for selection, wherein the processing of the respective channel sample then takes place in a processing cycle of all channels by said channel sample being selected in the analog multiplexer by a digital selection control signal for the analog/digital conversion and provided as analog selection signal at an output of the analog multiplexer and, after the respective channel provision area, being converted in an analog/digital converter, ~~characterized in that~~wherein an order of processing the channel sample detected in the respective first or second channel provision area ~~(31, 35)~~, which channel sample is provided by the analog selection signal ~~(15)~~ in an A/D conversion provision area (31) and then converted by the A/D converter, is calculated and determined individually for each channel sample by a channel controller ~~(4)~~.

3. A method as claimed in claim 2, ~~characterized in that~~wherein the calculations created in the channel controller ~~(4)~~ for the expiry of the multichannel analog/digital conversion are valid exclusively for detecting the channel samples in the first or second channel provision area ~~(32, 35)~~, wherein the detection of the channel sample present in the first or second channel provision area ~~(32, 35)~~ is respectively triggered by a first and second external detection signal ~~(42, 41)~~.

4. A method as claimed in claim 3, ~~characterized in that~~wherein a multichannel analog/digital conversion that continues through the detection of the channel sample present as analog signal in the first and/or second channel provision area ~~(31, 35)~~ is initiated in the A/D conversion provision area ~~(31)~~ by an external conversion request

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signal (40) which thus deposits a conversion request in the channel controller (4).

5. A method as claimed in claim 4, ~~characterized in that~~wherein additional data of the detected channel sample, which qualify an individual calculation of the time for processing a respectively detected channel sample in the channel controller (4), are notified to the channel controller (4) with the triggering of the conversion request by the additional external conversion request signal (40).

6. A method as claimed in claim 5, ~~characterized in that~~wherein the additional data, which are respectively notified to the channel controller (4) with the detected channel sample upon triggering of the associated conversion request signal (40), are an initial priority date, an increase rate of the priority per unit time, and an overall and a minimum validity period.

7. A method as claimed in claim 6, ~~characterized in that~~wherein the conversion request signals (40) are fed to the channel controller (4) together with the additional data on a data bus.

8. A method as claimed in claim 2, ~~characterized in that~~wherein the rules for individually calculating the time for processing a respectively detected channel sample are derived by means of metrics implemented in the channel controller.

9. A method as claimed in claim 2, ~~characterized in that~~wherein all signal-influencing times which lead to a shortening of the validity of a channel sample compared to its individual sampling period within the first and/or second channel (36), (37) from the first and/or second S/H element (1), (2) to the A/D S/H element (5) upstream of the A/D converter (6) are combined to form an invalidity period and with their invalidity period form a configuration variable that influences the metrics.

10. A method as claimed in claim 2, ~~characterized in that~~wherein one configuration variable that influences the metrics is the residual validity of a channel sample.

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11. A method as claimed in claim 2, ~~characterized in that~~wherein one configuration variable that influences the metrics is the minimum sampling period of a channel sample.

12. A method as claimed in claim 2, ~~characterized in that~~wherein the residual validity of a channel sample, which results from the currently remaining validity period of a respective channel sample present as analog signal in the respective assembly defining the analog signal, is determined in the form of a realized integrator assigned to this analog signal, wherein the integrator initial value which represents the validity period that has passed is presently monitored and, if this value exceeds the representing value of the overall validity ~~(61)~~, expiry of the validity period is ascertained, and otherwise its difference from the representing value of the overall validity ~~(61)~~ is the representing value of the remaining validity period.

13. A method as claimed in claim 2, ~~characterized in that~~wherein one configuration variable that influences the metrics is the randomly predefined priority of a channel sample.

14. A method as claimed in claim 2, ~~characterized in that~~wherein the respectively currently remaining validity period of the output signals of all the assemblies defining the analog signals in the first and second channel provision area ~~(31,35)~~ is known to the channel controller ~~(4)~~ and the remaining validity period is continuously determined anew in advance, and in that the next signal processing step in the respective assembly defining the analog signal is thus triggered by the channel controller ~~(4)~~.

15. A method as claimed in claim 2, ~~characterized in that~~wherein in the case of expiry of the validity period of one of the output signals of the assemblies defining the analog signals being determined by the channel controller ~~(4)~~ in the first and second channel provision area ~~(31,35)~~, an error signal ~~(39)~~ assigned to the respective output signal is output by the channel controller ~~(4)~~, or in the case of an available first S/H buffer memory or first further buffer memory ~~(26,43)~~ or second S/H buffer memory or second

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further buffer memory (29, 44) these output signals are buffer-stored by means of a first buffer memory control signal (17a) or first further buffer memory control signal (17b) or second buffer memory control signal (16a) or second further buffer memory control signal (16b).

16. A method as claimed in claim 2, ~~characterized in that~~wherein one configuration variable that influences the metrics is the buffer-storage that has taken place of a channel sample in a first and/or second S/H intermediate element (26), (29) and/or a first and/or second further buffer memory (43), (44).

17. (Cancel)

18. (Cancel)

19. (Cancel)

20. (Cancel)

21. A method as claimed in claim 1, ~~characterized in that~~wherein an output area (38) comprising the digital demultiplexer (7) and connected at least indirectly downstream of the A/D conversion provision area (31) comprising the analog/digital converter (6) at least indirectly provides at the respective outputs of the digital demultiplexer (7) the value converted for each channel by means of the demultiplexer selection signal (28) output by the channel controller (4), and in that these values are then buffer-stored in a first and second memory element (8), (9) assigned to the respective channel, said memory elements in each case likewise belonging to the output area, and read during activation of a respective first and second validity signal (23, 24).

22. A method as claimed in claim 1, ~~characterized in that~~wherein in times in which the assemblies contained in the A/D conversion provision area (31) and in the first and second channel provision area (32, 35) are not being used, wherein the analog/digital

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converter (6) is not performing any conversion and/or first and/or second S/H buffer
memories (26, 29) and/or first and/or second further buffer memories (43, 44) are not
storing any channel samples (13, 14) or analog selection signals (15), these are placed in
a state of low energy consumption so that the overall energy consumption is determined
by the respective sampling ratios of the A/D conversion signal (25) and/or the first and/or
second S/H buffer memory control signal (16a, 17a) and/or first and/or second further
buffer memory control signal (16b, 17b).

23. A method as claimed in claim 1, ~~characterized in that~~wherein the multichannel
analog/digital conversion takes place in the first and/or second channel (36, 37) and/or in
a further channel (45), wherein the further channel (45) is actuated by the channel
controller (4) by means of a supplementary control bus of the further channel (46).

24. A method as claimed in claim 1, ~~characterized in that~~wherein the first or second
analog signal (11, 12) or a further analog signal (47) is input to the first and/or second
channel (36, 37) and/or at least one further channel (45) for processing, wherein the
channels that are multiple-occupied by an analog signal are actuated all differently or
some differently by means of the associated external detection signals or S/H control
signals.

25. (Cancel)

26. An arrangement for multichannel analog/digital (A/D) conversion, wherein the
arrangement samples, by means of a respective first and second S/H (Sample & Hold)
element, in a first and second channel respectively in a first or second channel provision
area a first and second analog signal awaiting conversion and applies the respectively
stored sample value thereof as a channel sample to a first and second input of an analog
multiplexer for selection, wherein the arrangement then processes the respective channel
sample in a processing cycle of all channels by said channel sample being selected in the
analog multiplexer by a digital selection control signal for the analog/digital conversion
and provided as analog selection signal at an output of the analog multiplexer and, after

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the respective channel provision area, being converted in an analog/digital converter, ~~characterized in that~~wherein an order of processing the channel sample detected in the respective first or second channel provision area ~~(31, 35)~~, which channel sample is provided by the analog selection signal ~~(15)~~ in an A/D conversion provision area ~~(31)~~ and then converted by the A/D converter, is calculated and determined individually for each channel sample by a channel controller ~~(4)~~.

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